AISSMS COLLEGE OF ENGINEERING

ज्ञानम् सकलजनहिताय

Accredited by NAAC with "A+" Grade

DEPARTMENT OF E&TC ENGINEERING

VLSI DESIGN & TECHNOLOGY

TIME TABLE

CLASS: SE | **AY 2024-25 SEM I** | **W.E.F :-01-07-2024**

TIME / Day	08:15 AM to 09:15 AM	09:15 AM to 10:15 AM	10:15 AM to 10:30 AM	10:30 AM to 11:30 AM	11:30 AM to 12:30 PM	12:30 PM to 1:00 PM	01:00 PM to 02:00 PM	02:00 PM to 03:00 PM	3:00 PM to 4:00 PM
Monday	EC VBG 405	DC AAR 405	SHORT BREAK	DS VSN 405	FPGA VDN 405	LUNCH BREAK	M-III	Self Learning-B	
								Activity-C	
								LIBRARY HOUR-A	
Tuesday	DC AAR 405	EC VBG 405		VLSI-SE-EC-A-432-GDS			VLSI-SE-FPGA-A-452-VDN		Mentoring
				VLSI-SE-DS-B-456-VSN			VLSI-SE-FPGA-B- DC-437-AAR		
				VLSI-SE-ESD-C-437-DSB			VLSI-SE-EC-C-432-VBG		
Wednesday	DS VSN 405	M-III 405							
				VLSI-SE-DS-C-456-VSN			VLSI-SE-FPGA-B-452-VDN		
				VLSI-SE-ESD-A-437-GDS			VLSI-SE-FPGA-C- DC-437-AAR		
Thursday	FPGA VDN 405	M-III 405					DC AAR 405	Self Learning-C	Dept Meeting
				VLSI-SE-DS-A-456-VSN				Activity-A	
				VLSI-SE-ESD-B-437-GDS				LIBRARY HOUR-C	
Friday	DS VSN 425	FPGA VDN 425		VLSI-SE-FPGA-C-452-VDN			EC VBG 405	Self Learning-A	GFM Meeting
				VLSI-SE-FPGA-A- DC-437-NPM				Activity-B	
				VLSI-SE-EC-B-432-GDS				LIBRARY HOUR-C	

Subject:

ESD	ELECTRONIC SKILL DEVELOPMENT
EC	ELECTRONIC CIRCUITS
DS	DATA STRUCTURE
ELEC	ELECTRICAL CIRCUITS
DC	DIGITAL CIRCUITS
MIII	MATHEMATICS III
FPGA	FPGA based system design using Verilog

Faculty:

DSB/ GDS	DR.DS BORMANE /MS. GD SALUNKE
VBG/ GDS	MR.VB GAWAI /MS. GD SALUNKE
KBC	DR.KB CHAUDHARI
VSN	MS. VS NAVALE
VVD	DR.VV DESHMUKH
VDN	MS. VD NAGRALE

MS V D NAGRALE
Time-Table Incharge

Dr S B DHONDE
Head E&TC